GSV6201

DisplayPort 1.4 to HDMI 2.1 Converter with Embedded MCU

March, 2022

Preliminary Product Specification

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Glossary

DDC	Display Data Channel
EDID	Extended Display Identification Data
ESD	Electrostatic Discharge
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detect
I²C	Inter-Integrated Circuit
MCU	Microcontroller Unit
MISO	Master In Slave Out
MOSI	Master Out Slave In
OTP	One Time Programmable
PCM	Pulse Code Modulation
S/PDIF	Sony/Philips Digital Interface Format
SPI	Serial Peripheral Interface
TMDS	Transition Minimized Differential Signaling
SCDC	Status and Control Data Channel
CEC	Consumer Electronics Control
AUX	AUX_CH, DisplayPort Auxiliary Channel
DPCD	DisplayPort Configuration Data
Main-Link	Unidirectional channel stream from DPTX to DPRX
SDP	Secondary-data Packet
DDC/CI	VESA Display Data Channel/Command Interface
MCCS	Monitor Control Command Set (VESA)
DP	DisplayPort (VESA)
DPRX	DisplayPort Receiver
DPTX	DisplayPort Transmitter
DSC	Display Stream Compression
FEC	Forward Error Correction
HBR	DisplayPort High Bit Rate, HDMI High Bit-Rate Audio
MST	DisplayPort Multi-Stream Transport
SSC	Spread-Spectrum Clock

1. General Description

1.1 General Information

Gscoolink GSV6201 is a high-performance, low-power, USB Type-C Alternate Mode DisplayPort 1.4 to HDMI 2.1 converter. By integrating enhanced microcontroller, GSV6201 has created a cost-effective solution that provides time-to-market advantages. The DisplayPort Receiver supports up to 32.4Gbps (HBR3, 4-lane) and HDMI Transmitter supports up to 48Gbps (FRL, 12G4Lane). Integrated Power Delivery 3.0 controller handles Type-C CC interface for USB power management and DisplayPort mode entry. The superior architecture of GSV6201 provides economical smaller footprint solutions using QFN64, targeting applications of Type-C Docking, Type-C dongle and DP to HDMI cable.

GSV6201 supports all DisplayPort SDP packets and DSC stream pass-through to HDMI output. HDCP 1.4 and HDCP 2.2/2.3 are implemented in GSV6201 for both DisplayPort and HDMI TMDS and FRL mode. Color Space Conversion is supported at HDMI Tx in TMDS mode. Flexible implementations of Audio Insertion, Audio Extraction and SPDIF to I2S conversion are supported in GSV6201.

An internal Video Generator can be used to generate any uncompressed video timing defined in HDMI 2.1, such as 8K@60Hz, 8K@30Hz, 4K@120Hz, 480i@60Hz.

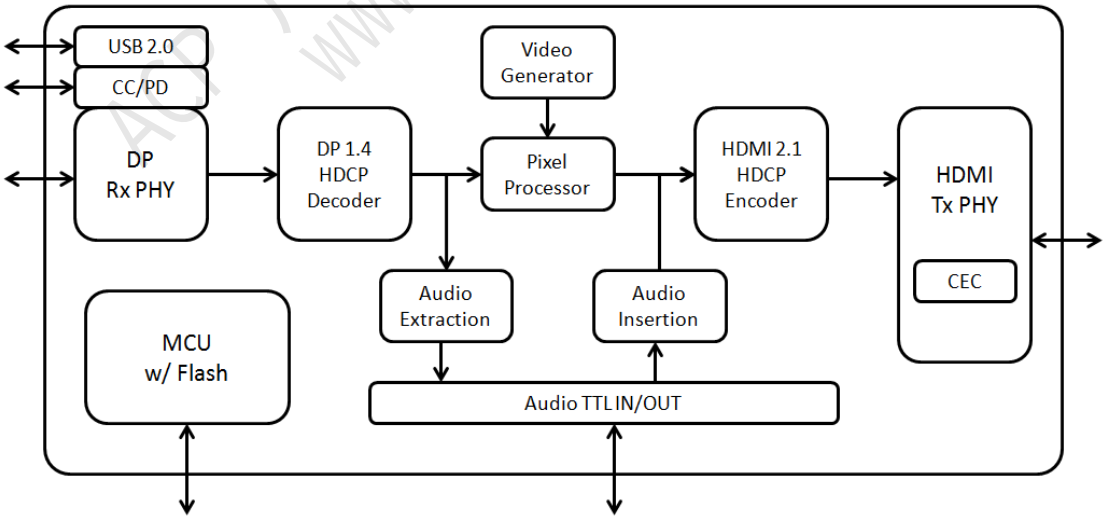


Figure 1. Top Diagram

The supported audio formats are listed in Table 1

Table 1. Supported Audio Format

Packet ID	Packet Type	Sampling Frequency (KHz)		
		32/44.1/48/88.2/ 96/176.4/192	256/352.8/384/ 512/705.6/768	64/128
0x02	Audio Sample Packet (LPCM and Compressed Audio)	Y		Y
0x07	One Bit Audio Sample Packet	Y		
0x08	DST Audio Packet	Y		
0x09	High Bit-rate Audio Stream Packet	Y	Y	

1.2 Features

1.2.1 DisplayPort Receiver

- Compliant with VESA DisplayPort 1.4a
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Support HBR3, HBR2, HBR and RBR (8.1/5.4/2.7/1.62 Gbps)
- Flexible 1/2/4 lane Main-Link configuration
- Programmable Adaptive Equalization
- Support Full-Link Training and No-Link Training
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Adaptive Sync/FreeSync
- Support Audio Extraction
- Support Horizontal Blanking Expansion up to 4K@120Hz format
- Support Forward Error Correction (FEC)
- Embedded arbitrary EDID and MCCS
- Support Spread Spectrum Clock (SSC)

1.2.2 HDMI Transmitter

- Compliant with HDMI 2.1, HDMI 2.0b, HDMI 1.4b
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Data rate up to 48Gbps (FRL 12Gbps/4 Lane)
- Programmable Voltage Swing, Slew-Rate and Pre-emphasis
- Support AC-coupling on TMDS
- Support Color Space Converter in HDMI 2.0 mode

- Support HDR (HDR10/HDR10+/Dolby Vision/HLG)
- Support Variable Refresh Rate (VRR)/FreeSync
- Support DSC encoded stream pass-through
- Hardware CEC Engine for Low Level protocol decoding
- 5V tolerance on DDC/HPD/CEC pins

1.2.3 USB Type-C Interface

- USB Power Delivery 3.0 Compliant controller
- 3 Configuration Channels (CC) with built-in Rp/Rd resistors
- Dual Role Power Port (DRP)
- Fast Role Swap
- USB 2.0 full-speed billboard enumeration

1.2.4 Audio Input/Output

- I2S and SPDIF Audio Extraction from DisplayPort Rx
- I2S/SPDIF Audio Insertion to HDMI Tx
- SPDIF/I2S/HBR/DSD/TDM Format Supported for Audio Extraction and Insertion
- SPDIF to I2S Conversion using single TTL bus in Bi-direction

1.2.5 System Features

- Embedded internal MCU
- External pins of Flash QSPI interface
- External 25MHz Crystal required
- Available Pins for UART/Timer/GPIO
- Temperature Sensor Monitoring Circuit

1.3 Chip Application Modes

1.3.1 DP to HDMI Conversion

Based on the DisplayPort input and output requirement, GSV6201 can dynamically switch between FRL and HDMI 2.0 mode for the best compatibility in 8K/4K/2K timings. Audio extraction can be applicable if required.

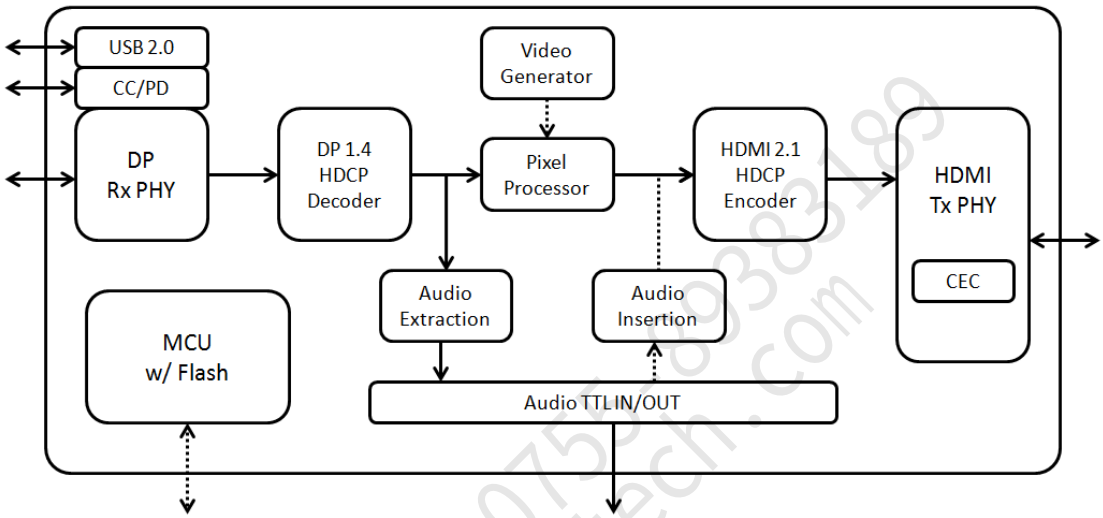


Figure 2. Switch Between FRL/TMDS Conversion

1.3.2 Audio Insertion for HDMI Tx

I2S/SPDIF audio stream and DisplayPort Rx video can be inserted into HDMI Tx.

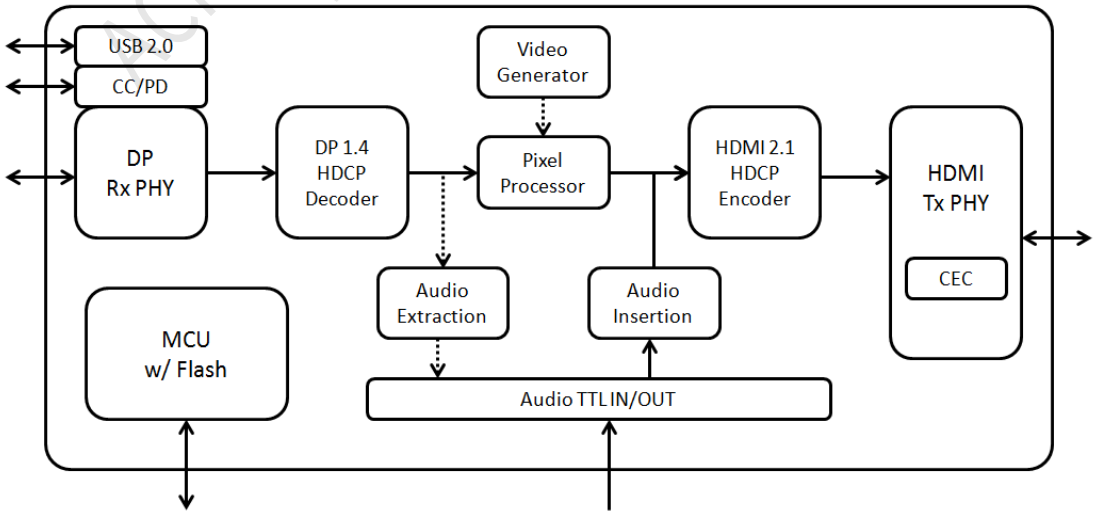


Figure 3. Audio Insertion Application

1.4 Audio Bus Output Configuration

When one group of audio bus is configured as output, I2S and SPDIF are output at the same time. General configuration of pin settings is shown below:

Table 2. I2S/SPDIF Audio Extraction

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Output	I2S Data, default stereo channels
AUD_D1	SDATA[1]	Output	I2S Data, 3/4 channels
AUD_D2	SDATA[2]	Output	I2S Data, 5/6 channels
AUD_D5	LRCLK/WS	Output	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Output	Fixed to 64Fs
MCLK	Sys Clock	Output	Selected from 128Fs/256Fs/384Fs/512Fs

1.5 Audio Bus Input Configuration

When Audio Bus is set to Input, either I2S or SPDIF can be selected. It should be noted that external MCLK is required in I2S audio insertion mode.

For SPDIF input, GSV6201 can detect Sampling Frequency and automatically update it into Channel Status with GSV software. For I2S input, software designer needs to indicate the input sampling frequency in software.

General application modes are listed below.

Table 3. Stereo I2S Input

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Input	I2S Data, default stereo channels
AUD_D5	LRCLK/WS	Input	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Input	Fixed to 64Fs
MCLK	Sys Clock	Input	Selected from 128Fs/256Fs/384Fs/512Fs

Table 4. SPDIF Input

Pin Name	Alias	Direction	Description
AUD_D0	SPDIF	Input	SPDIF channel

Table 5. 8-Channel I2S Input

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Input	I2S Data, default stereo channels
AUD_D1	SDATA[1]	Input	I2S Data, 3/4 channels
AUD_D2	SDATA[2]	Input	I2S Data, 5/6 channels
AUD_D5	LRCLK/WS	Input	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Input	Fixed to 64Fs
MCLK	Sys Clock	Input	Selected from 128Fs/256Fs/384Fs/512Fs

2. Pin Description

2.1 Pin Diagram

QFN64 Pin definition is defined as below.

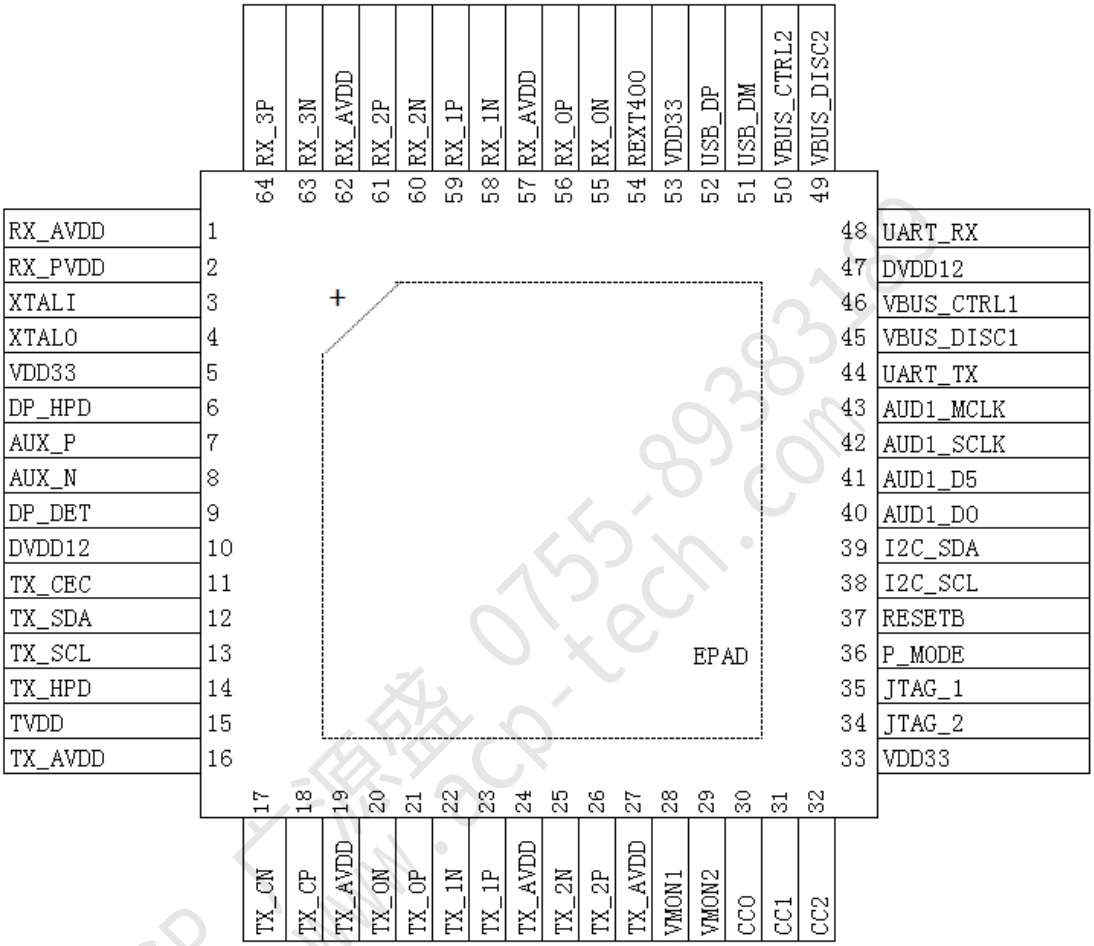


Figure 4. GSV6201 QFN64 Pin Diagram

2.2 Pin Description

Table 6. QFN64 Pin Description

Pin Name	Direction	Pin No.	Description
DisplayPort Rx Pins			
DP_DET	I	9	RX DP Detection PAD
DP_HPD	I/O	6	RX HPD PAD, can be used as GPIO Input in Type-C Application

AUX_P	I/O	7	RX AUX_P PAD, Type-C SBU_P
AUX_N	I/O	8	RX AUX_N PAD, Type-C SBU_N
DRX_0N	I	55	RX Negative Main-Link differential data input [0]
DRX_0P	I	56	RX Positive Main-Link differential data input [0]
DRX_1N	I	58	RX Negative Main-Link differential data input [1]
DRX_1P	I	59	RX Positive Main-Link differential data input [1]
DRX_2N	I	60	RX Negative Main-Link differential data input [2]
DRX_2P	I	61	RX Positive Main-Link differential data input [2]
DRX_3N	I	63	RX Negative Main-Link differential data input [3]
DRX_3P	I	64	RX Positive Main-Link differential data input [3]
USB Type-C Pins			
USB_DP	I/O	52	USB 2.0 D+ Pin
USB_DM	I/O	51	USB 2.0 D- Pin
VMON1	I/O	28	VBus Monitor Pin 1
VMON2	I/O	29	VBus Monitor Pin 2
CC0	I/O	30	Type-C CC Pin0, standalone CC pin
CC1	I/O	31	Type-C CC Pin1, combination with CC Pin2(32)
CC2	I/O	32	Type-C CC Pin2, combination with CC Pin1(31)
Power/Ground Pins			
DVDD12	Power	10,47	Digital 1.2V voltage power supply
TVDD	Power	15	Analog 3.3V voltage power supply for TX Port
VDD33	Power	5,33,53	Digital 3.3V voltage power supply
RX_AVDD	Power	1,57,62	Analog 1.2V voltage power supply for RX Port
TX_AVDD	Power	16,19,24, 27	Analog 1.2V voltage power supply for TX Port
RX_PVDD	Power	2	PLL 1.2V voltage power supply for RX port
REXT400	Power	54	External 1.8V Power supply in production, External 400 ohm resistors to 3.3V Power supply in application
HDMI Tx Pins			
TX_CEC	I/O	11	TXA CEC Pin, can be used as GPIO Output in Type-C
TX_SDA	I/O	12	TXA DDC SDA Pin
TX_SCL	O	13	TXA DDC SCL Pin
TX_HPD	I	14	TXA HPD PAD

TX_CN	O	17	TXA Negative TMDS clock output/ differential data output [3]
TX_CP	O	18	TXA Positive TMDS clock output/ differential data output [3]
TX_0N	O	20	TXA Negative TMDS differential data output [0]
TX_0P	O	21	TXA Positive TMDS differential data output [0]
TX_1N	O	22	TXA Negative TMDS differential data output [1]
TX_1P	O	23	TXA Positive TMDS differential data output [1]
TX_2N	O	25	TXA Negative TMDS differential data output [2]
TX_2P	O	26	TXA Positive TMDS differential data output [2]
Digital pins			
I2C_SDA	I/O	39	Digital IO for I2C Data Alternate 1: GPIO8
I2C_SCL	I/O	38	Digital IO for I2C Clock Alternate 1: GPIO9
UART_TX	I/O	44	Default: UART_TX for internal MCU Alternate 1: Digital IO PAD for Audio Data0 Alternate 2: GPIO7 Alternate 3: QSPI Flash D1 pin
VBUS_DISC1	I/O	45	Default: Type-C VBus Discovery Pin 1 Alternate 1: Digital IO PAD for Audio Data1 Alternate 2: GPIO10 Alternate 3: UART TX
VBUS_CTRL1	I/O	46	Default: Type-C VBus Control Pin 1 Alternate 1: Digital IO PAD for Audio Data2 Alternate 2: GPIO11 Alternate 3: UART RX
UART_RX	I/O	48	Default: UART_RX for internal MCU Alternate 1:Digital IO PAD for Audio Data5 Alternate 2: QSPI Flash D0 pin Alternate 3: GPIO6 Alternate 4: TX CEC
VBUS_DISC 2	I/O	49	Default: Type-C VBus Discovery Pin 2 Alternate 1:Digital IO PAD for Audio SCLK Alternate 2: QSPI Flash SCK pin Alternate 3: GPIO5 Alternate 4: Advanced Timer 2

VBUS_CTRL 2	I/O	50	Default: Type-C VBus Control Pin 2 Alternate 1:Digital IO PAD for Audio MCLK Alternate 2: QSPI Flash CSB pin Alternate 3: GPIO4 Alternate 4: Advanced Timer 1
RESETB	I	37	Reset Pin. Low for reset state, High for functional state.
XTALI	I/O	3	25M Crystal Input
XTALO	I/O	4	25M Crystal output
P_MODE	I	36	Internal MCU Boot Option High = QSPI Flash boot Low = External MCU boot
JTAG_1	I/O	35	TCK, Internal MCU programming pin
JTAG_2	I	34	TMS, Internal MCU programming pin
AUD1_MCLK	I/O	43	Digital IO PAD QSPI_CSB for QSPI Flash connection (this pin has no audio input/output function)
AUD1_SCLK	I/O	42	Digital IO PAD QSPI_SCK for QSPI Flash connection (this pin has no audio input/output function)
AUD1_D5	I/O	41	Digital IO PAD QSPI_D0 for QSPI Flash connection (this pin has no audio input/output function)
AUD1_D0	I/O	40	Digital IO PAD QSPI_D1 for QSPI Flash connection (this pin has no audio input/output function)

3. Electrical Specifications

3.1 Timing Information

3.1.1 Power Up and Reset Timing Diagrams

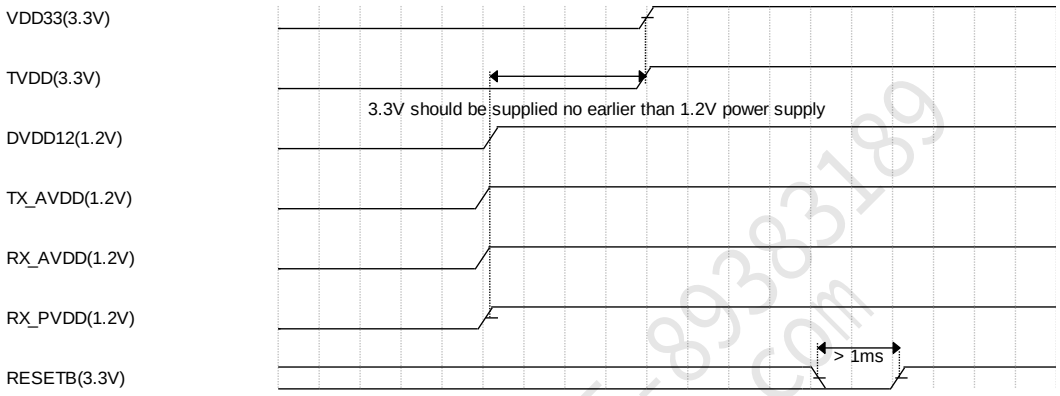


Figure 5. Power Up Sequence

3.1.2 I2C Timing Diagrams

The I2C bus uses 8-bit page address and 16-bit register address. ACK should be provided per 8-bit transaction. For every register, 8-bit data will be accessed. The device address is 0xB0 in 8-bit.

The I2C write timing is shown below.

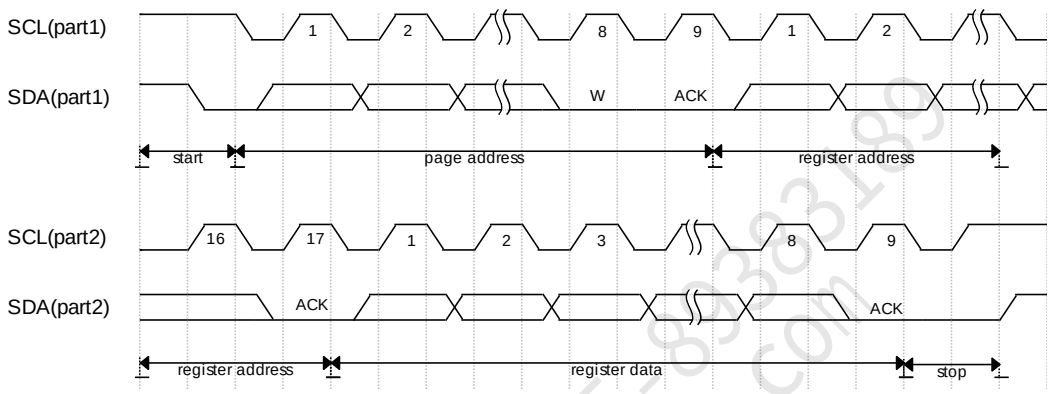


Figure 6. I2C Timing Diagram(Write)

The I2C read timing is shown below.

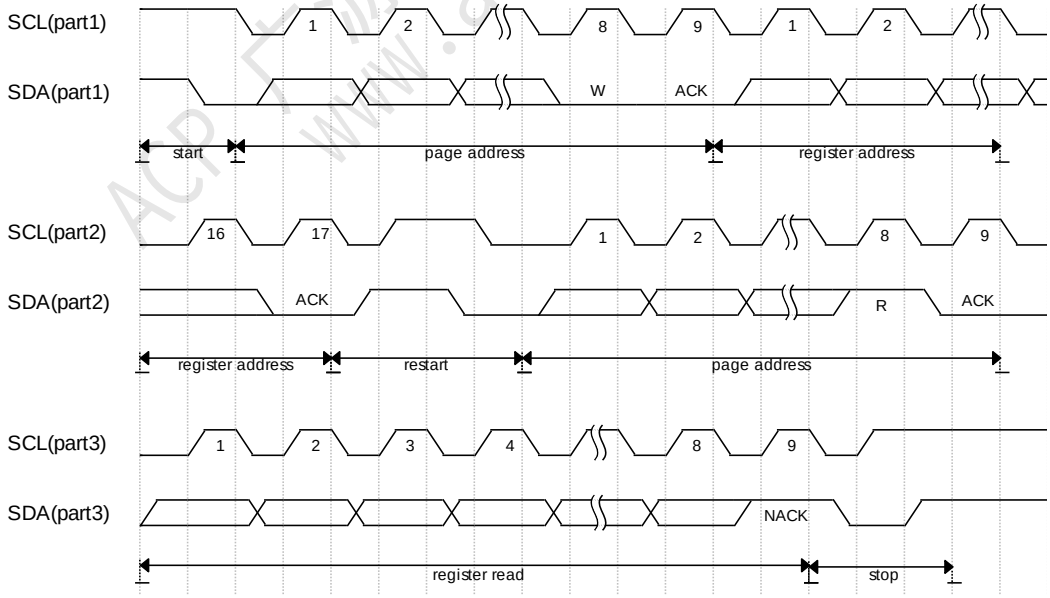


Figure 7. I2C Timing Diagram(Read)

3.2 Operating Conditions

3.2.1 Temperature Conditions

GSV6201's operation temperature range is -20 ºC to 85 ºC. The maximum junction temperature is at 125 ºC. GSV6201 embeds internal temperature sensor for junction temperature read back.

3.2.2 Electrical Conditions

Table 7. Absolute Maximum Ratings

Power Domain	Minimum	Typical	Maximum
DVDD33	-0.5V	3.3V	5.0V
TVDD	-0.5V	3.3V	5.0V
DVDD12	-0.5V	1.2V	1.8V
RX_AVDD	-0.5V	1.2V	1.8V
TX_AVDD	-0.5V	1.2V	1.8V
RX_PVDD	-0.5V	1.2V	1.8V

Table 8. Functional Operation Conditions

Power Domain	Minimum	Typical	Maximum
DVDD33	3.0V	3.3V	3.6V
TVDD	3.0V	3.3V	3.6V
DVDD12	1.08V	1.2V	1.32V
RX_AVDD	1.08V	1.2V	1.32V
TX_AVDD	1.08V	1.2V	1.32V
RX_PVDD	1.08V	1.2V	1.32V

3.2.3 Audio Pin Conditions

GSV6201's Audio TTL pins can tolerate 2.8V~3.6V as logic HIGH.

3.2.4 I2C Conditions

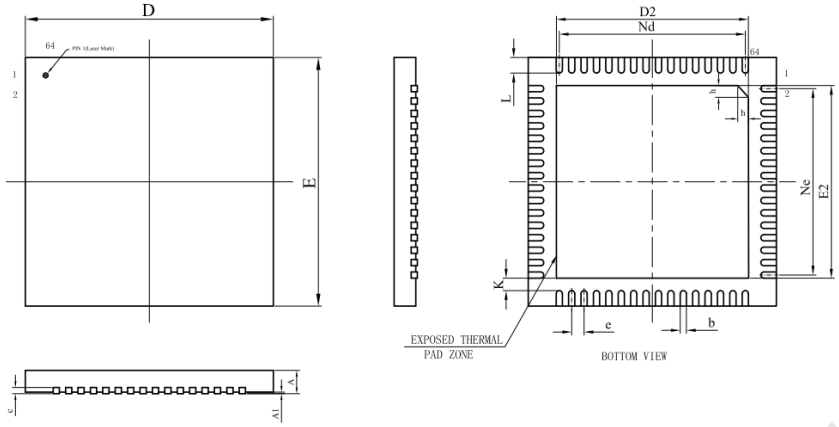
GSV6201's I2C maximum SCL frequency is 400KHz.

3.3 HDMI Transmitter

Table 9. TMDS DC and AC Characteristics

Item	Value
Single-Ended High Level Voltage Range: Data Channels 0,1,2	TVDD - 400mV ~ TVDD + 10mV
Single-Ended Low Level Voltage Range: Data Channels 0,1,2	TVDD - 1000mV ~ TVDD - 400mV
Single-Ended High Level Range: Clock Channel	TVDD - 400mV ~ TVDD + 10mV
Single-Ended Low Level Voltage Range: Clock Channel	TVDD - 1000mV ~ TVDD - 400mV
Single-Ended Swing Voltage: Data Channels 0,1,2	400mV~600mV
Single-Ended Swing Voltage: Clock Channel	200mV~600mV

4. Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	7.90	8.00	8.10
D2	6.10	6.20	6.30
e	0.40BSC		
Nd	6.00BSC		
E	7.90	8.00	8.10
E2	6.10	6.20	6.30
Ne	6.00BSC		
L	0.45	0.50	0.55
K	0.20	—	—
h	0.30	0.35	0.40
载体尺寸 (mil)	258*258		

Figure 8. Package Dimensions (QFN64)

5. Ordering Guide

Table 10. Ordering Information

Part Number.	Temperature Range	Package Description	Packing Type
GSV6201	−20°C to +85°C	QFN64	Tray

6. Revision History

Table 11. Revision history

Revision No.	Description	Date
V0.1	Draft Initial Version for internal review.	Apr 28, 2022
V0.2	Package information update to QFN64	Jun 28, 2022
V0.3	Pin mapping update	Jul 18, 2022
V0.4	Correct Power up sequence	Jul 22, 2022
V0.5	Modify content to mass production version.	Aug 4, 2022
V0.6	Modify pin position of I2C/RESETB/P_MODE	Sep 5, 2022
V0.7	Modify audio support feature	Sep 15, 2022
V0.8	Correct CEC/Rx HPD GPIO description	Oct 14, 2022
V0.9	Correct DVDD12 pin 39 declaration	Oct 19, 2022
V0.10	Clarify External Flash definition	Jan 3, 2023
V0.11	Correct AUD1 bus pin description	Feb 8, 2023
V1.0	Add Power Information	Mar 3, 2023
V1.1	Add description about VideoGen	Apr 17, 2023

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