GSV6502

1 In to 2 Out HDMI 2.1 Splitter with Embedded MCU

April, 2022

Preliminary Product Specification

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CONTENTS

FIGURES

TABLES

Glossary

DDC	Display Data Channel
EDID	Extended Display Identification Data
ESD	Electrostatic Discharge
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detect
I^2C	Inter-Integrated Circuit
MCU	Microcontroller Unit
MISO	Master In Slave Out
MOSI	Master Out Slave In
OTP	One Time Programmable
PCM	Pulse Code Modulation
S/PDIF	Sony/Philips Digital Interface Format
SPI	Serial Peripheral Interface
TMDS	Transition Minimized Differential Signaling
SCDC	Status and Control Data Channel
CEC	Consumer Electronics Control
DDC/CI	VESA Display Data Channel/Command Interface
MCCS	Monitor Control Command Set (VESA)
DSC	Display Stream Compression
FEC	Forward Error Correction
HBR	HDMI High Bit-Rate Audio
SSC	Spread-Spectrum Clock

1. General Description

1.1 General Information

Gscoolink GSV6502 is a high-performance, low-power 1 In to 2 Out HDMI 2.1 to HDMI 2.1 splitter. By integrating enhanced microcontroller based on RISC-V, GSV6502 has created a cost-effective solution that provides time-to-market advantages. GSV6502's HDMI Receiver and HDMI Transmitter supports up to 48Gbps (FRL, 12G/4Lane). The superior architecture of GSV6502 provides economical smaller footprint solutions using QFN88, targeting applications of Consumer and ProAV.

GSV6502 supports all uncompressed HDMI input video/audio decoding/encoding and DSC stream pass-through to HDMI output. HDCP 1.4 and HDCP 2.2/2.3 are implemented in GSV6502 for both HDMI Input and Output in HDMI 2.0 and FRL mode. HDR-SDR Conversion, Deinterlacer, Downscaler, 444-420 Conversion, Color Space Conversion are supported in HDMI Tx in HDMI 2.0 and FRL mode. Flexible implementations of Audio Insertion, Audio Extraction and SPDIF to I2S conversion are supported in GSV6502. Embedded CEC engine enables flexible remote control of the entire HDMI signal chain.

An internal Video Generator can be used to generate any uncompressed video timing defined in HDMI 2.1, such as 8K@60Hz, 8K@30Hz, 4K@120Hz, 480i@60Hz.

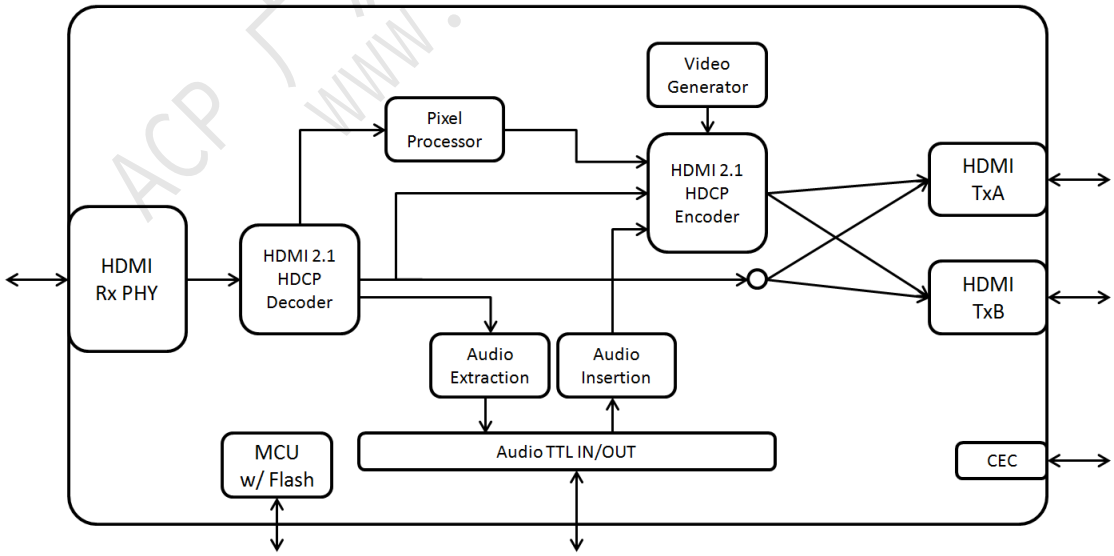


Figure 1. Top Diagram

The supported audio formats are listed in Table 1

Table 1. Supported Audio Format

Packet ID	Packet Type	Sampling Frequency (KHz)		
		32/44.1/48/88.2/ 96/176.4/192	256/352.8/384/ 512/705.6/768	64/128
0x02	Audio Sample Packet (LPCM and Compressed Audio)	Y		Y
0x07	One Bit Audio Sample Packet	Y		
0x08	DST Audio Packet	Y		
0x09	High Bit-rate Audio Stream Packet	Y	Y	

1.2 Features

1.2.1 HDMI Receiver

- Compliant with HDMI 2.1, HDMI 2.0b, HDMI 1.4b
- Compliant with HDCP 2.2/2.3 and HDCP 1.4 in repeater/receiver mode
- Data rate up to 48Gbps (FRL 12Gbps/4 Lane)
- Programmable Adaptive Equalization
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Variable Refresh Rate (VRR), FreeSync, G-Sync
- Support ALLM
- Support Forward Error Correction (FEC)
- Support DSC pass-through for compressed input timing
- Embedded arbitrary EDID (up to 512 bytes)
- 5V tolerance on DDC/HPD pins

1.2.2 HDMI Transmitter

- Compliant with HDMI 2.1, HDMI 2.0b, HDMI 1.4b
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Data rate up to 48Gbps (FRL 12Gbps/4 Lane)
- Programmable Voltage Swing, Slew-Rate and Pre-emphasis
- Support AC-coupling on TMDS
- Support Color Space Converter in FRL and HDMI 2.0 mode
- Support HDR (HDR10/HDR10+/Dolby Vision/HLG)
- Support Variable Refresh Rate (VRR), FreeSync, G-Sync

- Support ALLM
- Support DSC encoded stream pass-through
- Hardware CEC Engine for Low Level protocol decoding
- 5V tolerance on DDC/HPD/CEC pins

1.2.3 Pixel Processor

- HDR to SDR conversion for HDR10, HDR10+, HLG and Low Latency DolbyVision
- Color Space conversion
- YCbCr 444-420 timing conversion
- Downscaler with selectable 2/3/4/8/16/32 ratio
- Deinterlacer for interlaced timing

1.2.4 Audio Input/Output

- I2S and SPDIF Audio Extraction from HDMI Rx
- I2S/SPDIF Audio Insertion to HDMI Tx
- SPDIF/I2S/HBR/DSD/TDM Format Supported for Audio Extraction and Insertion
- SPDIF to I2S Conversion using single TTL bus in Bi-direction

1.2.5 System Features

- Optional External MCU (via I2C)/ Internal MCU mode for chip control
- Embedded MCU and External Flash
- External pins of Flash QSPI interface
- External 25MHz Crystal required
- Available Pins for UART/Timer/GPIO
- Temperature Sensor Monitoring Circuit

1.3 Chip Application Modes

1.3.1 HDMI 1to2 Repeater with audio extraction

The default 1to2 repeater application mode of GSV6502 is that 2 HDMI outputs copy the same TMDS/FRL stream from HDMI input. Other than HDMI input lane frequency, GSV6502 HDMI Outputs have an advanced feature of generating a shared secondary FRL/TMDS lane frequency. For example, HDMI input timing is 4K@60Hz using FRL 12G/4Lane, and secondary lane frequency is set to HDMI 2.0 TMDS mode. Any of the 2 HDMI outputs can choose either default 4K@60Hz using FRL 12G/4Lane, or secondary 4K@60Hz using HDMI 2.0 TMDS mode.

Meanwhile, Audio extraction can be applicable if required.

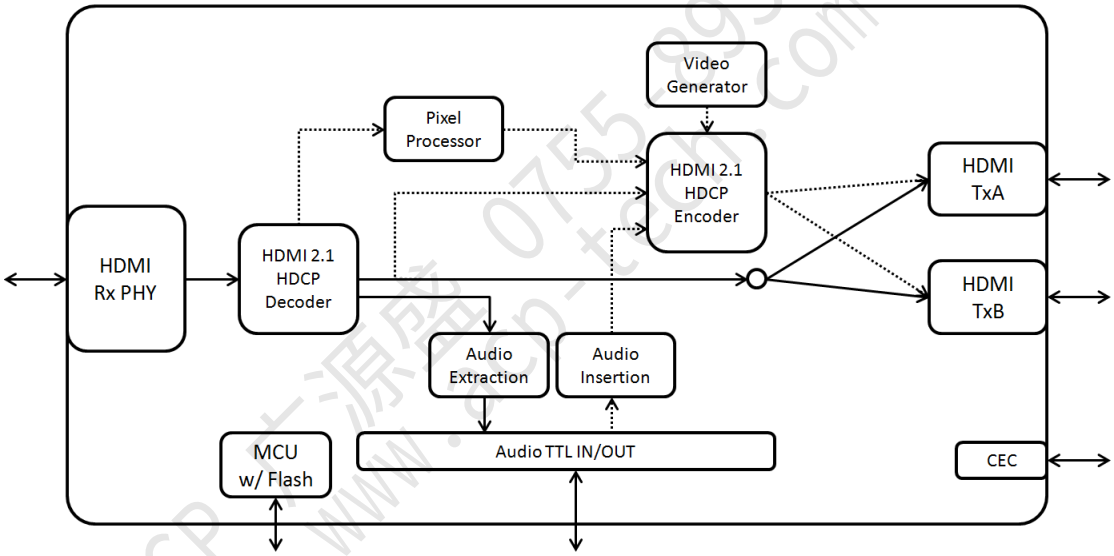


Figure 2. HDMI to HDMI 1to2 repeater with audio extraction

1.3.2 HDMI 1to2 Repeater with compatible HDMI 1.4 timing

Within bandwidth limitation, GSV6502 can keep input stream consistent and intact, while dynamically switch output between FRL and HDMI 2.0 mode for the best compatibility. For example, when FRL12G/4Lane 4K@60Hz timing is input, GSV6502 can convert to HDMI 2.0 or FRL 6G/3Lane, FRL 6G/4Lane, FRL 8G/4Lane, FRL 10G/4Lane, FRL 12G/4Lane as output. During HDMI output mode switch, HDMI input stream will not be disturbed.

GSV6502 can also support fixed output FRL rate, regardless of HDMI input mode. For

example, when HDMI 2.0 4K@30Hz is input, GSV6502 can convert it to FRL 10G/4Lane output. And when FRL 8G/4Lane 4K@120Hz is input, GSV6502 can still maintain FRL 10G/4Lane output with timing conversion.

And using pixel processor, For any HDMI 2.1 uncompressed timing, while most HDMI outputs can copy HDMI 2.1 input stream for HDMI 2.1 downstream devices. The secondary HDMI 1.4 or DVI timing with SDR color can be generated as output stream for any compatible HDMI 1.4 or DVI downstream devices.

Meanwhile, Audio extraction can be applicable if required.

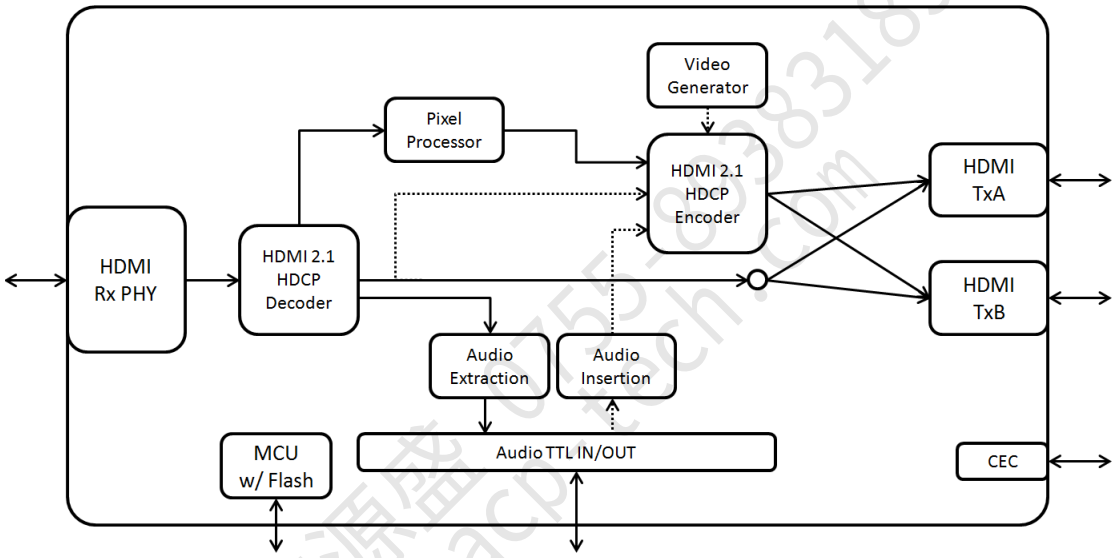


Figure 3. HDMI 1to2 repeater with compatible HDMI 1.4 timing

1.3.3 Audio Insertion for HDMI Tx

I2S/SPDIF audio stream and HDMI Rx video can be inserted into HDMI Tx. While video stream is the same, audio stream can be chosen between HDMI Rx audio or inserted audio.

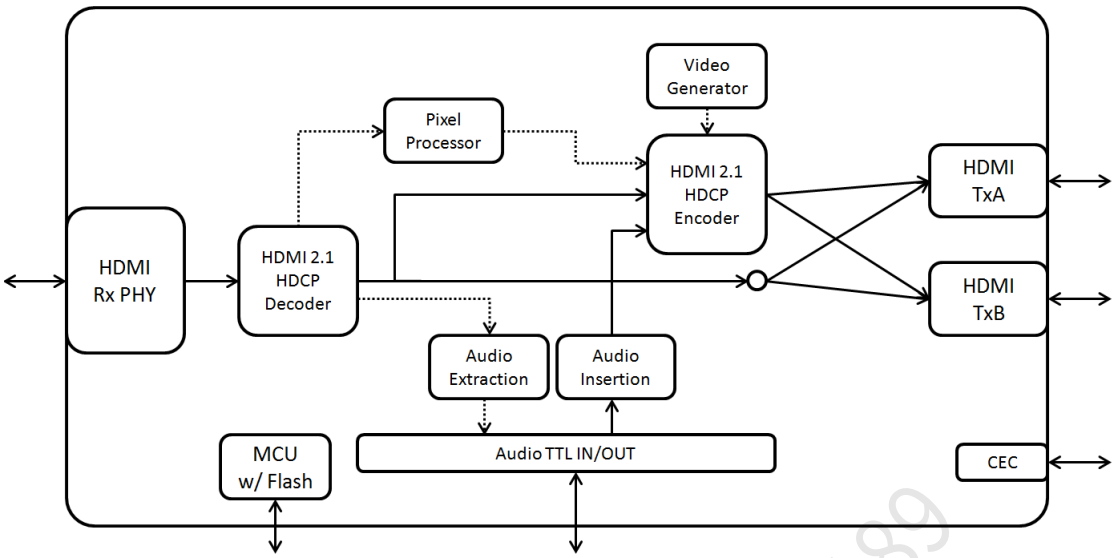


Figure 4. Audio Insertion Application

1.4 Audio Bus Output Configuration

When one group of audio bus is configured as output, I2S and SPDIF are output at the same time. General configuration of pin settings is shown below:

Table 2. I2S/SPDIF Audio Extraction

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Output	I2S Data, default stereo channels
AUD_D5	LRCLK/WS	Output	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Output	Fixed to 64Fs
MCLK	Sys Clock	Output	Selected from 128Fs/256Fs/384Fs/512Fs

For HBR application, it is also capable of sending out SPDIF in 4-pin mode.

Table 3. HBR Audio Extraction in SPDIF

Pin Name	Alias	Direction	Description
AUD_D0	SPDIF[0]	Output	SPDIF Data[0], 1/2 channels

1.5 Audio Bus Input Configuration

When Audio Bus is set to Input, either I2S or SPDIF can be selected. It should be noted that external MCLK is required in I2S audio insertion mode.

For SPDIF input, GSV6502 can detect Sampling Frequency and automatically update it into Channel Status with GSV software. For I2S input, software designer needs to indicate the input sampling frequency in software.

General application modes are listed below.

Table 4. Stereo I2S Input

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Input	I2S Data, default stereo channels
AUD_D5	LRCLK/WS	Input	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Input	Fixed to 64Fs
MCLK	Sys Clock	Input	Selected from 128Fs/256Fs/384Fs/512Fs

Table 5. SPDIF Input

Pin Name	Alias	Direction	Description
AUD_D0	SPDIF	Input	SPDIF channel

Table 6. 8-Channel I2S Input

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Input	I2S Data, default stereo channels
AUD_D5	LRCLK/WS	Input	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Input	Fixed to 64Fs
MCLK	Sys Clock	Input	Selected from 128Fs/256Fs/384Fs/512Fs

1.6 Audio Bus Input/Output Bi-Direction Configuration

When bi-direction is needed for a single audio bus, stereo audio insertion and extraction can be simultaneously supported.

Table 7. I2S Audio Insertion and Extraction in Bi-Direction

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Output	I2S Data, default stereo channels
AUD_D5	LRCLK/WS	Input	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Input	Fixed to 64Fs
MCLK	Sys Clock	Input	Selected from 128Fs/256Fs/384Fs/512Fs

2. Pin Description

2.1 Pin Diagram

QFN88 Pin definition is defined as below.

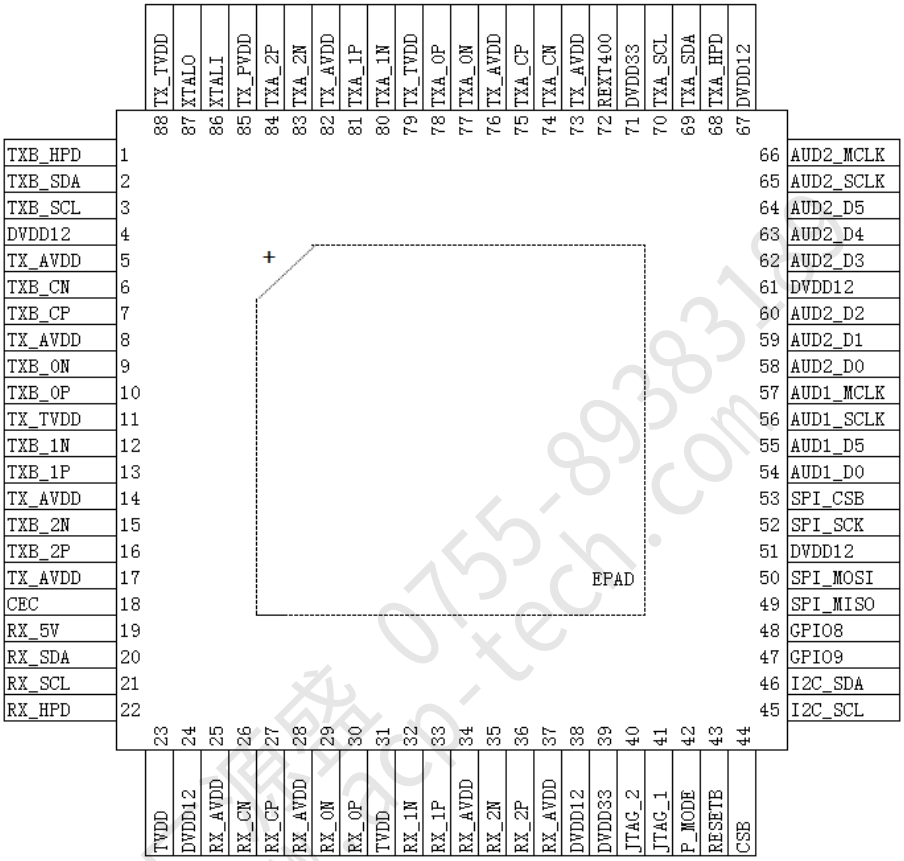


Figure 5. GSV6502 QFN88 Pin Diagram

2.2 Pin Description

Table 8. QFN88 Pin Description

Pin Name	Direction	Pin No.	Description
HDMI Rx Pins			
RX_5V	I	19	RX 5V Detection PAD
RX_HPD	I/O	22	RX HPD PAD
RX_SDA	I/O	20	RX DDC SDA PAD
RX_SCL	I/O	21	RX DDC SCL PAD

RX_CN	I	26	RX Negative TMDS differential data input [3]/ TMDS clock differential input
RX_CP	I	27	RX Positive TMDS differential data input [3]/ TMDS clock differential input
RX_0N	I	29	RX Negative TMDS differential data input [0]
RX_0P	I	30	RX Positive TMDS differential data input [0]
RX_1N	I	32	RX Negative TMDS differential data input [1]
RX_1P	I	33	RX Positive TMDS differential data input [1]
RX_2N	I	35	RX Negative TMDS differential data input [2]
RX_2P	I	36	RX Positive TMDS differential data input [2]
Power/Ground Pins			
DVDD12	Power	4,24,38,51, 61,67,	Digital 1.2V voltage power supply
TVDD	Power	23,31,	Analog 3.3V voltage power supply for RX Port
TX_TVDD	Power	11,79,88	Analog 3.3V voltage power supply for TX Port
DVDD33	Power	39,71,	Digital 3.3V voltage power supply
RX_AVDD	Power	25,28,34,37	Analog 1.2V voltage power supply for RX Port
TX_AVDD	Power	5,8,14,17, 73,76,82	Analog 1.2V voltage power supply for TX Port
TX_PVDD	Power	85	PLL 1.2V voltage power supply for TX port
REXT400	Power	72	External 400 ohm resistors to 3.3V Power supply
HDMI Tx Pins			
TXA_SDA	I/O	69	TXA DDC SDA Pin
TXA_SCL	O	70	TXA DDC SCL Pin
TXA_HPD	I	68	TXA HPD PAD
TXA_CN	O	74	TXA Negative TMDS clock output/ differential data output [3]
TXA_CP	O	75	TXA Positive TMDS clock output/ differential data output [3]
TXA_0N	O	77	TXA Negative TMDS differential data output [0]
TXA_0P	O	78	TXA Positive TMDS differential data output [0]
TXA_1N	O	80	TXA Negative TMDS differential data output [1]
TXA_1P	O	81	TXA Positive TMDS differential data output [1]
TXA_2N	O	83	TXA Negative TMDS differential data output [2]
TXA_2P	O	84	TXA Positive TMDS differential data output [2]
TXB_SDA	I/O	2	TXB DDC SDA Pin

TXB_SCL	O	3	TXB DDC SCL Pin
TXB_HPD	I	1	TXB HPD PAD
TXB_CN	O	6	TXB Negative TMDS clock output/ differential data output [3]
TXB_CP	O	7	TXB Positive TMDS clock output/ differential data output [3]
TXB_0N	O	9	TXB Negative TMDS differential data output [0]
TXB_0P	O	10	TXB Positive TMDS differential data output [0]
TXB_1N	O	12	TXB Negative TMDS differential data output [1]
TXB_1P	O	13	TXB Positive TMDS differential data output [1]
TXB_2N	O	15	TXB Negative TMDS differential data output [2]
TXB_2P	O	16	TXB Positive TMDS differential data output [2]
CEC	I/O	18	TX CEC Pin
Digital pins			
I2C_SDA	I/O	46	Digital IO for I2C Data
I2C_SCL	I/O	45	Digital IO for I2C Clock
GPIO8	I/O	48	GPIO8 for internal MCU control
GPIO9	I/O	47	GPIO9 for internal MCU control
SPI_CSB	I/O	53	QSPI_CSB for QSPI Flash connection
SPI_SCK	I/O	52	QSPI_SCK for QSPI Flash connection
SPI_MOSI	I/O	50	QSPI_MOSI for QSPI Flash connection
SPI_MISO	I/O	49	QSPI_MISO for QSPI Flash connection
AUD2_D0	I/O	58	Digital IO PAD Default: Data0 of Audio Bus 2 Alternate 1: GPIO7 for internal MCU control Alternate 2: UART_RX for internal MCU control
AUD2_D1	I/O	59	Digital IO PAD Default: Data1of Audio Bus 1 Alternate 1: GPIO10 for internal MCU control Alternate 2: UART_TX for internal MCU control
AUD2_D2	I/O	60	Digital IO PAD Default: Data2 of Audio Bus 1 Alternate 1: GPIO11 for internal MCU control Alternate 2: UART_RX for internal MCU control

AUD2_D3	I/O	62	Digital IO PAD Default: Data3 of Audio Bus 1 Alternate 1: GPIO12 for internal MCU control Alternate 2: Advanced Timer1 for internal MCU control
AUD2_D4	I/O	63	Digital IO PAD Default: Data4 of Audio Bus 1 Alternate 1: GPIO13 for internal MCU control Alternate 2: Advanced Timer2 for internal MCU control
AUD2_D5	I/O	64	Digital IO PAD for Audio Data5 Default: Data5 of Audio Bus 2 Alternate 1: GPIO6 for internal MCU control Alternate 2: UART_TX for internal MCU control Alternate 3: CEC
AUD2_SCLK	I/O	65	Digital IO PAD for Audio SCLK Default: SCLK of Audio Bus 2 Alternate 1: GPIO5 for internal MCU control Alternate 2: ADV_TIM2 for internal MCU control
AUD2_MCLK	I/O	66	Digital IO PAD for Audio MCLK Default: MCLK of Audio Bus 2 Alternate 1: GPIO4 for internal MCU control Alternate 2: ADV_TIM1 for internal MCU control
RESETB	I	43	Reset Pin. Low for reset state, High for functional state.
CSB	I	44	CSB: Low for I2C selection
XTALI	I/O	86	25M Crystal Input
XTALO	I/O	87	25M Crystal output
JTAG_1	I/O	41	TCK, Internal MCU programming pin Alternate: AVMUTE interrupt pin
JTAG_2	I/O	40	TMS, Internal MCU programming pin Alternate: INT interrupt pin
P_MODE	I	42	Internal MCU Boot Option High = QSPI Flash boot Low = External MCU boot

AUD1_D0	I/O	54	Digital IO PAD Default: Data0 of Audio Bus 1 Alternate 1: GPIO0 for internal MCU control Alternate 2: UART_RX for internal MCU control
AUD1_D5	I/O	55	Digital IO PAD Default: Data5 of Audio Bus 1 Alternate 1: GPIO1 for internal MCU control Alternate 2: UART_TX for internal MCU control
AUD1_SCLK	I/O	56	Digital IO PAD Default: SCLK of Audio Bus 1 Alternate 1: GPIO3 for internal MCU control Alternate 2: ADV_TIM2 for internal MCU control
AUD1_MCLK	I/O	57	Digital IO PAD Default: MCLK of Audio Bus 1 Alternate 1: GPIO2 for internal MCU control Alternate 2: ADV_TIM1 for internal MCU control

3. Electrical Specifications

3.1 Timing Information

3.1.1 Power Up and Reset Timing Diagrams

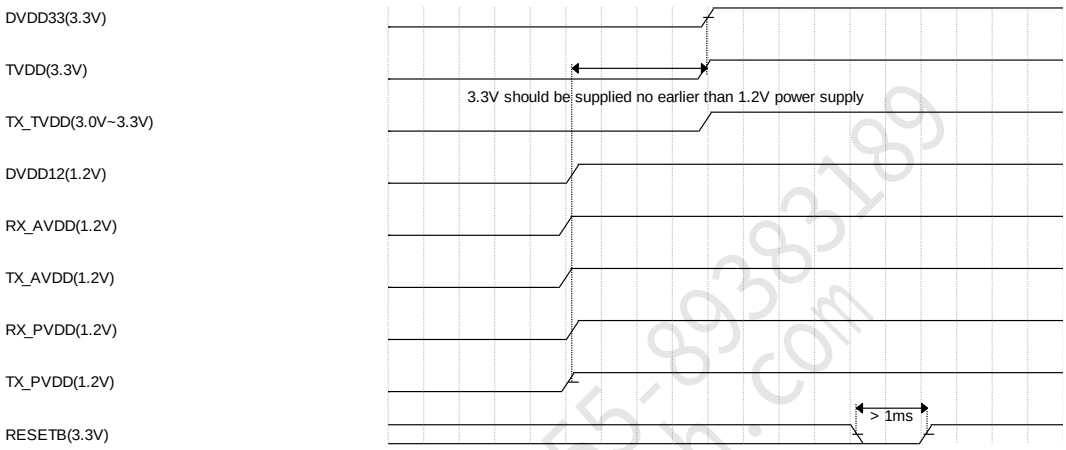


Figure 6. Power Up Sequence

3.1.2 I2C Timing Diagrams

The I2C bus uses 8-bit page address and 16-bit register address. ACK should be provided per 8-bit transaction. For every register, 8-bit data will be accessed. The device address is 0xB0 in 8-bit.

The I2C write timing is shown below.

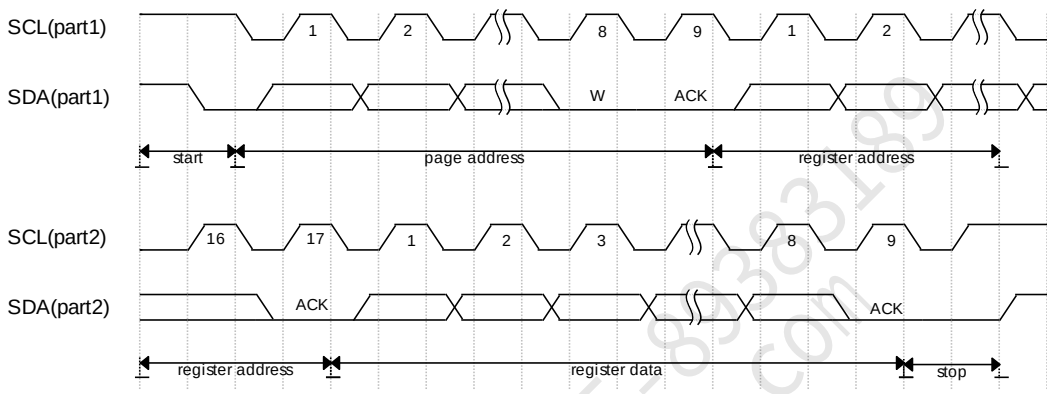


Figure 7. I2C Timing Diagram(Write)

The I2C read timing is shown below.

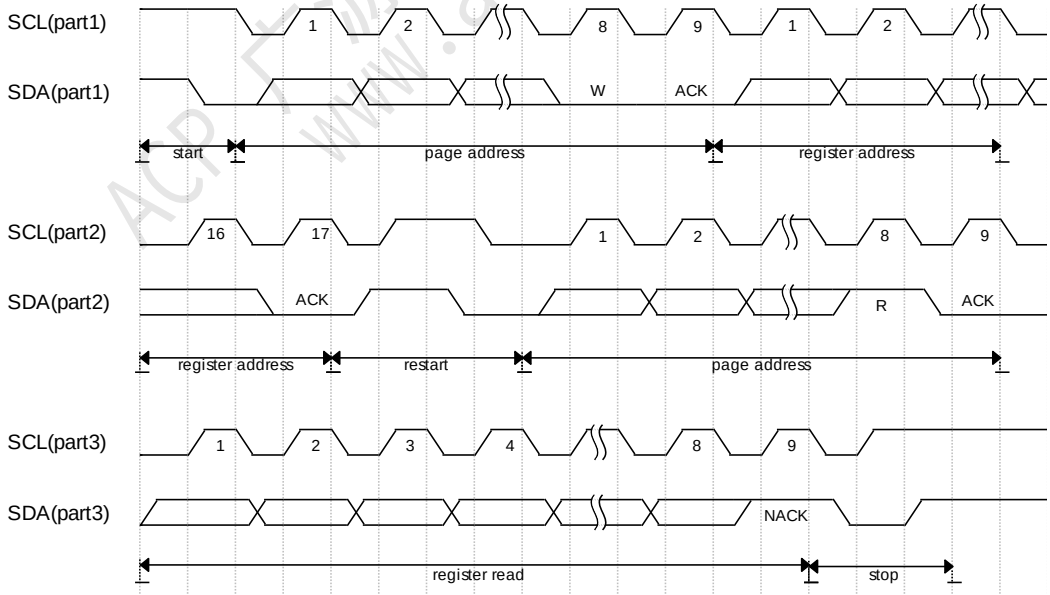


Figure 8. I2C Timing Diagram(Read)

3.1.3 I2S Timing Diagrams

I2S standard timing is shown as below, which is the default I2S timing of audio input/output.

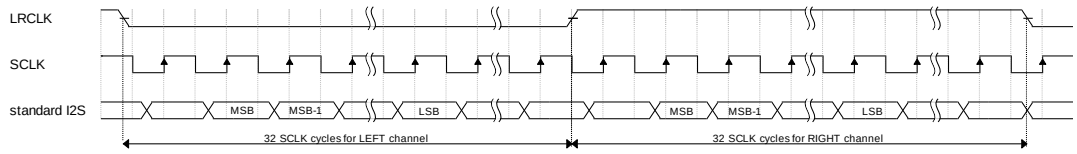


Figure 9. I2S Standard Timing Diagram

I2S left-justified timing is shown as below, which is can be tuned by register configuration.

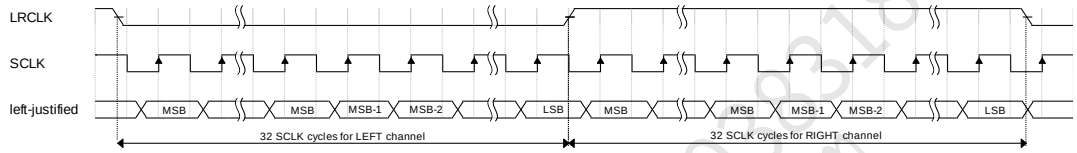


Figure 10. I2S Left-Justified Timing Diagram

I2S right-justified timing is shown as below, which is can be tuned by register configuration.

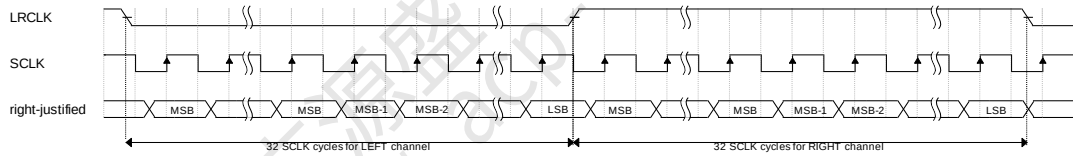


Figure 11. I2S Right-Justified Timing Diagram

3.2 Operating Conditions

3.2.1 Temperature Conditions

GSV6502's operation temperature range is -20 ºC to 85 ºC. The maximum junction temperature is at 125 ºC. GSV6502 embeds internal temperature sensor for junction temperature read back.

3.2.2 Electrical Conditions

Table 9. Absolute Maximum Ratings

Power Domain	Minimum	Typical	Maximum
DVDD33	-0.5V	3.3V	5.0V
TVDD	-0.5V	3.3V	5.0V
TX_TVDD	-0.5V	3.3V	5.0V
DVDD12	-0.5V	1.2V	1.8V
RX_AVDD	-0.5V	1.2V	1.8V
TX_AVDD	-0.5V	1.2V	1.8V
TX_PVDD	-0.5V	1.2V	1.8V

Table 10. Functional Operation Conditions

Power Domain	Minimum	Typical	Maximum
DVDD33	3.0V	3.3V	3.6V
TVDD	3.0V	3.3V	3.6V
TX_TVDD	3.0V	3.3V	3.6V
DVDD12	1.08V	1.2V	1.32V
RX_AVDD	1.08V	1.2V	1.32V
TX_AVDD	1.08V	1.2V	1.32V
TX_PVDD	1.08V	1.2V	1.32V

3.2.3 Audio Pin Conditions

GSV6502's Audio TTL pins can tolerate 2.8V~3.6V as logic HIGH.

3.2.4 I2C Conditions

GSV6502's I2C maximum SCL frequency is 400KHz.

3.2.5 Crystal Oscillator Conditions

GSV6502's crystal oscillator input should be <300 ppm, EF<0.7, CL=18pF,ESR=50.

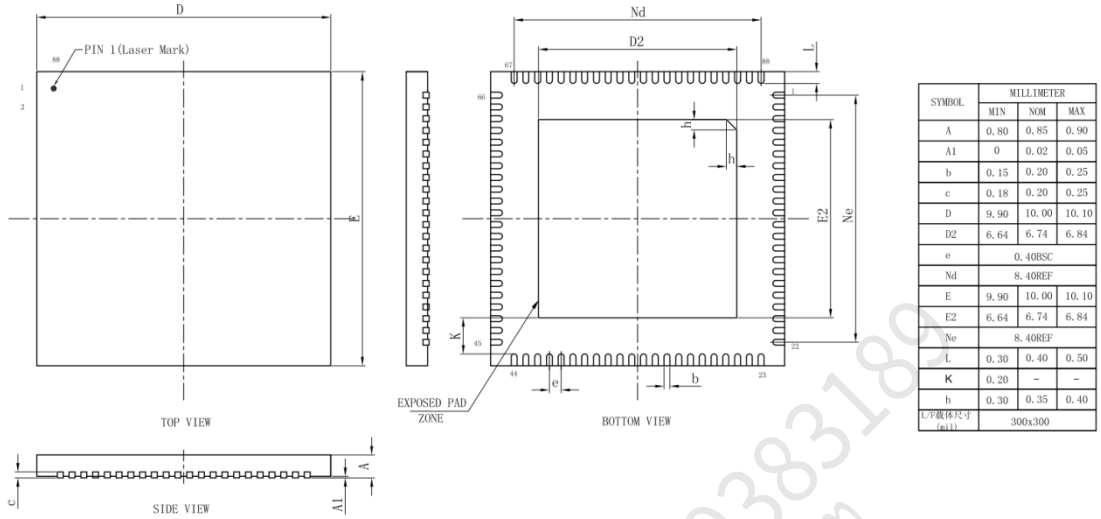
3.3 HDMI Transmitter

Table 11. TMDS DC and AC Characteristics

Item	Value
Single-Ended High Level Voltage Range: Data Channels 0,1,2	TVDD - 400mV ~ TVDD + 10mV
Single-Ended Low Level Voltage Range: Data Channels 0,1,2	TVDD - 1000mV ~ TVDD - 400mV

Single-Ended High Level Range: Clock Channel	TVDD - 400mV ~ TVDD + 10mV
Single-Ended Low Level Voltage Range: Clock Channel	TVDD - 1000mV ~ TVDD - 400mV
Single-Ended Swing Voltage: Data Channels 0,1,2	400mV~600mV
Single-Ended Swing Voltage: Clock Channel	200mV~600mV

4. Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	9.90	10.00	10.10
D2	6.64	6.74	6.84
e	0.40BSC		
Nd	8.40REF		
E	9.90	10.00	10.10
E2	6.64	6.74	6.84
Ne	8.40REF		
L	0.30	0.40	0.50
K	0.20	-	-
h	0.30	0.35	0.40
L/F载体尺寸 (mil)	300x300		

Figure 12. Package Dimensions (QFN88)

5. Ordering Guide

Table 12. Ordering Information

Part Number.	Temperature Range	Package Description	Packing Type
GSV6502	−20°C to +85°C	QFN88	Tray

6. Revision History

Table 13. Revision history

Revision No.	Description	Date
V0.1	Draft Initial Version for internal review.	Apr 28, 2022
V0.2	Clarify External Flash definition	Jan 3, 2023
V1.0	Add Power Information	Mar 3, 2023
V1.1	Separate TX_TVDD pins in pin list, add I2S timing table and crystal requirement	Apr 12, 2023

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